	National Institute of Technology Meghalaya An Institute of National Importance	CURRICULUM

Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**VI**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 324	**DSP Systems & Architectures**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	To study digital representation of Various number systems		CO1	Describe the different representation of number systems
	To understand the redundant and residue number system and application		CO2	Concept of redundant number and residue number system and implementation concept
	To understand the concept of binary addition, multiplication and division circuits		CO3	Familiarization of different adder architectures
	To understand concept of floating point arithmetic		CO4	Familiarization of different architectures of multipliers and dividers
	To understand the concept of floating point arithmetic circuits		CO5	Familiarization with floating point number representation in digital domain and architectures of floating point circuits
			CO6	

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**2**	**-**	**-**	**1**	**1**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**
2	CO2	-	-	-	**3**	**2**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**
3	CO3	-	-	**3**	**2**	**2**	**3**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**2**
4	CO4	-	-	-	-	-	-	**3**	**3**	**-**	**-**	**-**	**-**	**2**	**3**	**2**
5	CO5	-	-	-	-	-	-	-	**3**	**2**	**-**	**-**	**-**	**3**	**3**	**3**
6	CO6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

SYLLABUS

No.	Content	Hours	COs
I	**DSP Integrated Circuits** Introduction, Digital Signal Processing, Standard Digital Signal Processors, Application Specific ICs for DSP, DSP Systems, DSP System Design, Integrated Circuit Design.	**08**	**CO1**
II	**Digital Signal Processing** The Fourier Transformation, The Z Transformation, Sampling of Analog Signals, Selection of Sampling Frequency, Signal Processing Systems, Difference Equation, Frequency Response, Transfer Function, Filter Structure, DFT and FFT, Adaptive DSP Algorithm, DCT.	**10**	**CO2**
III	**DSP Algorithm** DSP Systems, Precedence Graph, SFG in Precedence Form, Difference Equation, Computation Graph, Equivalence Transformation, Interleaving and Pipelining, Algorithm Transformation, Mapping Technique, Scheduling, Scheduling Formulation, Resource Allocation, Resource Scheduling, Interpolator	**10**	**CO3**
IV	**DSP System Architectures** Standard DSP Architecture, TMS 32series, Ideal DSP Architecture, Multiprocessor, Multicomputer, Systolic Array, Wave Front Array, Shared Memory Architecture.	**08**	**CO4**
VII			
	Total Hours	**36**	

Essential Readings

1. L. Wanhammer, “DSP Integrated Circuits”, Academic Press, 1st Edition, 1999
2. U. Meyer-Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer Publications, 1st Edition, 2001

Supplementary Readings

1. M. D. Ercegovac, Digital Arithmetic, The Morgan Kaufmann Series in Computer Architecture and Design. 1st Edition, 2003.
2. D. A. Patterson and J. L. Hennessy, Computer Organization and Design, Morgan Kaufmann Publishers Inc. San Francisco, 5 th Edition, 2014.
3. A. V. Oppenheim, R.W. Schafer, “Discrete Time Signal Processing”, Prentice Hall Publication, 3rd Edition, 2014.